Microwave On-Wafer Characterization of Three-Port Devices using Shield-Based Test-Fixtures

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Abstract— **The capability of shield-based test-fixture design used in conjunction with three-port device measurements is demonstrated. The reduction of forward coupling and common-ground parasitics facilitates simple de-embedding that can easily be applied to multi-port measurements. The procedure is detailed and the capability of the method is demonstrated with gigahertz device measurements.**

I. Introduction

On-wafer device characterization is an important enabler for high-performance first-try RF integrated circuits. With the high-paced development, device models often lack behind IC technologies and direct on-wafer measurement is of high importance. However, traditional two-port measuring configurations, e.g. common-source and common-emitter, are not appropriate in circuit configurations where no device terminals are DC and AC grounded. As a possible solution, multi-port measurements facilitate independent biasing of all device terminals. In practice, three-port measurements are often sufficient, e.g. for BJT/MOSFET characterization.

Although three-port measurements have become more convenient with multi-port test-sets and network analyzers, there are still some critical issues that relate to the environment of the *device under test* (DUT). Silicon technology, which has established itself as a leading RFIC contender, suffers from large parasitics of interconnects and the semiconducting substrate [1]. For the on-wafer characterization of physically small devices, this leads to large measuring inaccuracies although the *vector network analyzer* (VNA) has been properly calibrated to the probe tips. Hence, we need to apply additional correction in the form of de-embedding. However, a multi-port generalization of common de-embedding methods [2], [3] is too complicated for practical use. In this paper, we extend the shield-based test-fixture design method [4] to three-port measurements. The low forward coupling of the test-fixture facilitates low-complexity de-embedding without reducing accuracy. We detail the measuring method and illustrate its capability with gigahertz device and circuit measurements. An RF CMOS circuit example demonstrates how the use of two-port measurements give strongly misleading results while three-port measurements succeed.

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II. 3-Port Measurements with 2-Port VNA

This section outlines a method that can be used to perform three-port S-parameter measurements with a two-port VNA. The method is based on work by Tippet, Speciale, and Dropkin [5], [6] and combines three different two-port measurements into corresponding three-port parameters for the DUT. As illustrated in Fig. 1a, each two-port S-parameter set is measured with an arbitrary impedance Z_n on the "third" port n which is not connected to the VNA. Ideally, this impedance is 50Ω, but this is not achievable due to parasitics of the intervening chip-to-coaxial interface, cables, and bias-tee's. By moving the termination around, we obtain a total of three two-port S-parameters sets, named $M1$ (port 1 to port 2), $M2$ (port 1 to port 3), and $M3$ (port 2 to port 3) respectively. This measurement series is illustrated for an MOSFET in Fig. 1c and the obtained results are

$$\begin{bmatrix} s_{11}^{M1} & s_{12}^{M1} \\ s_{21}^{M1} & s_{22}^{M1} \end{bmatrix}, \begin{bmatrix} s_{11}^{M2} & s_{13}^{M2} \\ s_{31}^{M2} & s_{33}^{M2} \end{bmatrix}, \text{ and } \begin{bmatrix} s_{22}^{M3} & s_{23}^{M3} \\ s_{32}^{M3} & s_{33}^{M3} \end{bmatrix} \quad (1)$$

Each of these measurements is calibrated by conventional two-port methods using straight and bended standards. After a successful two-port calibration, the above sets of two-port S-parameters are normalized according to Table I.

TABLE I
Reference impedance versus measurement.

	Reference impedance [Ω]		
Measurement	Port 1	Port 2	Port 3
$M1$	50	50	Z_3
$M2$	50	Z_2	50
$M3$	Z_1	50	50

To be able to combine the three measuring sets, they need to be re-normalized to the same reference impedance on the same port. Hence, we need to know the "third" port impedances Z_1, Z_2, and Z_3. With each two-port calibration, these impedances are estimated using a thru standard as shown in Fig. 1b. Once, these "third" port impedances are known we can re-normalize all measurements to Z_1 (port 1), Z_2 (port 2), and Z_3 (port 3) by employing standard re-normalization techniques [6]. Note that we cannot re-normalize directly to 50Ω for all ports. The re-normalized

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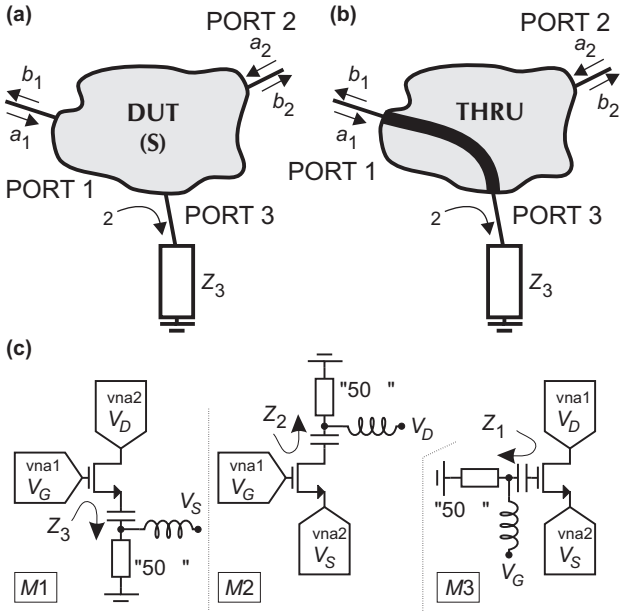

Fig. 1. Illustration of (a) two-port configuration with port 3 terminated, (b) thru standard used to measure the impedance of the third port, and (c) setup of the three required two-port measurements of an MOSFET.

measurements are denoted $M1'$, $M2'$, and $M3'$. As they refer to the same reference impedance for each port, a three-port matrix can be formed as

$$\mathbf{S}'_{ms} = \begin{bmatrix} \frac{s_{11}^{M1'}+s_{11}^{M2'}}{2} & s_{12}^{M1'} & s_{13}^{M2'} \\ s_{21}^{M1'} & \frac{s_{22}^{M1'}+s_{22}^{M3'}}{2} & s_{23}^{M3'} \\ s_{31}^{M2'} & s_{32}^{M3'} & \frac{s_{33}^{M2'}+s_{33}^{M3'}}{2} \end{bmatrix} \quad (2)$$

where we average redundant measurements. As a final step, the matrix $\mathbf{S}'_{ms}$ is re-normalized back to the nominal reference impedance $Z_0 = 50\Omega$ for all ports [6]. This gives us $\mathbf{S}_{ms}$ which is the final result.

III. Test-Fixture and De-Embedding Strategy

The accuracy of the three-port measurement depends on (i) careful VNA handling and calibration as well as (ii) careful design of the test-fixture holding the DUT. The latter is particularly critical for silicon-based technologies where high-complexity de-embedding is needed to subtract test-fixture effects [2], [3]. Recently, shield-based design methodologies [4] have introduced numerous benefits, including (i) effective mitigation of port-port leakage due to improved common ground, (ii) high area-efficiency due to full scalability of test-fixture parasitics, and (iii) relieved de-embedding requirements since the number of significant parasitics is reduced. In this work, we have extended the shield-based methodology to a three-port scenario as shown in Fig. 2. As for the two-port case [4], Fig. 3 shows that the worst-case port-port coupling exhibits negligible values. Further, the low-loss ground shield effectively mitigates the impedance between DUT and ground pads.

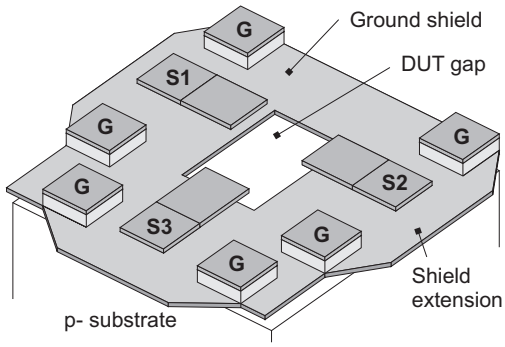

Fig. 2. Basic three-port shield-based test-fixture.

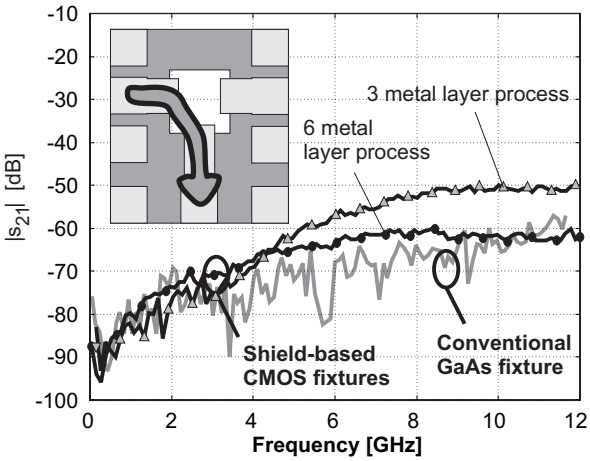

Fig. 3. Port-port coupling of shield-based three-port test-fixtures.

Due to these properties, the shield-based three-port test-fixture can accurately be represented by the simple equivalent model shown in Fig. 4a. Note that each 4-component ladder-section (for each port) could be reduced to just two components – a parallel and a series impedance. However, the chosen representation allows us to separate probe/pad effects from fixture effects and, hence, use symmetry considerations to evaluate the achieved de-embedding accuracy [4]. The series parasitics are extracted using simple and full short standards, while simple and full open standards are used to extract the parallel effects. The open and short standards are fabricated by removing the DUT from a test-fixture and replacing it with the standards shown conceptually in Fig. 4b.

Using the three-port measuring approach described earlier, we obtain the 3×3 S-parameter matrix, $\mathbf{S}_{ms}$, including DUT and test-fixture effects. To de-embed the measurement, the scattering matrix is converted into impedance pa-

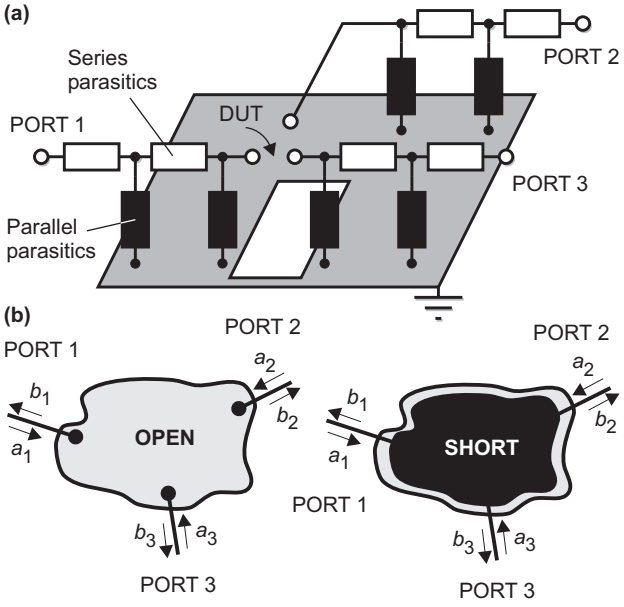

Fig. 4. Illustration of (a) test-fixture model, (b) de-embedding standards.

rameters as

$$\mathbf{Z}_{ms} = Z_0 \cdot (\mathbf{I} + \mathbf{S}_{ms})\,(\mathbf{I} - \mathbf{S}_{ms})^{-1} \quad (3)$$

where $\mathbf{I}$ is the 3×3 identity matrix. For each calibrated port n, we measure the simple/full short and open standards, thereby obtaining the impedances and admittances $Z_{ss,n}$, $Z_{fs,n}$ (with $Z_{ss,n}$ subtracted), $Y_{so,n}$, and $Y_{fo,n}$ (with $Y_{so,n}$ subtracted). These may be obtained from measured one-port reflection coefficients [4]. We then form diagonal matrices

$$\mathbf{Z}_{ss} = \begin{bmatrix} Z_{ss,1} & 0 & 0 \\ 0 & Z_{ss,2} & 0 \\ 0 & 0 & Z_{ss,3} \end{bmatrix} \quad (4)$$

for cases 'ss', 'fs', 'so', and 'fo'. The actual DUT Y-parameters are then extracted as

$$\mathbf{Y}_{DUT} = \left(\left((\mathbf{Z}_{ms} - \mathbf{Z}_{ss})^{-1} - \mathbf{Y}_{so} \right)^{-1} - \mathbf{Z}_{fs} \right)^{-1} - \mathbf{Y}_{fo} \quad (5)$$

and can be converted into any desired two-port format.

IV. Measurements and Verification

To illustrate the capability of the method, three-port measurements have been conducted on a 200×0.25 μm MOSFET device. The shield-based test-fixture and de-embedding standards, shown in Fig. 5, were fabricated in a 6-metal layer 0.25 μm CMOS technology. The pads fit 150 μm-pitch GSG probes. By rotating the chip, the short and full open/short standards are accessible by all probes. Although the structure consumes a relatively large die area, recall that the shown standards can be used to de-embed other measurements as well. Since probe overlap on the standards is critical for the probe-die impedance, the asymetrical full standards should only be probed from the intended side.

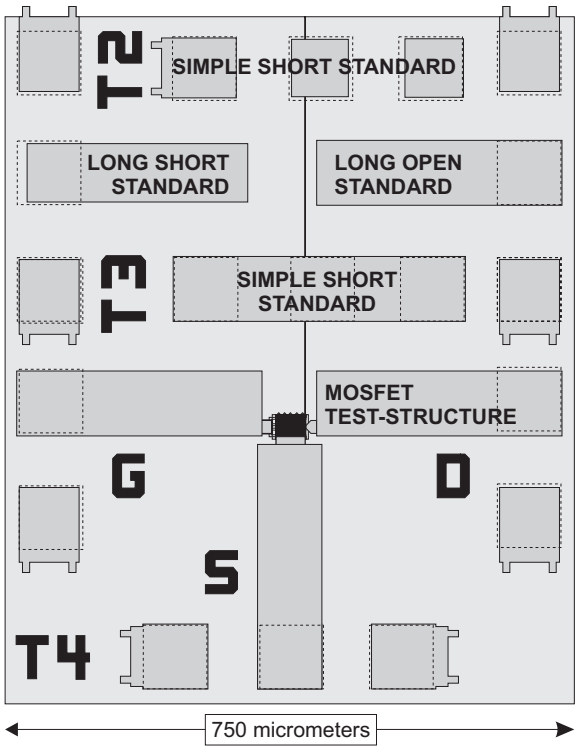

Fig. 5. On-wafer three-port test structures.

For each two-port calibration of our HP8510C VNA system, the accuracy was carefully evaluated using an open stub verification standard available on our *impedance standard substrate* (ISS). As no bended reference attenuator is available on the ISS, a bended thru standard was used to verify the transmission calibration. For the present measuring range (45 MHz to 12 GHz), we use a SOLR calibration [7] to ensure the best accuracy near open and short terminations. This method also relieves the accuracy requirements for the bended thru standard. In Fig. 6, the measured and normalized MOSFET input reflection coefficient is plotted for two different two-port calibrations (zero bias). Very good agreement is achieved indicating a good measuring/calibration reliability and good consistency between bended and straight thru standards.

The complete set of scattering parameters for the considered MOSFET in strong inversion saturation are shown in Fig. 7. All curves are smooth which indicates that proper compensation for the reflection at the third port has been accomplished. As expected, the low frequency phase difference between s_{21} and s_{31} is 180°. The input reflection cor-

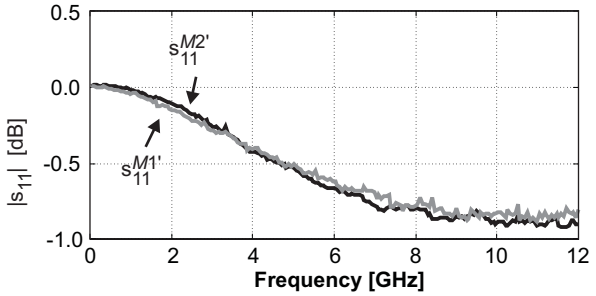

Fig. 6. Verification measurements for port-port consistency.

responds to a capacitor (s_{11}) and at low frequency there is good isolation between gate and drain/source (s_{13} and s_{12}). Although the test-structure consumes a significant amount of die space, it facilitates an evaluation of the MOSFET in all possible configurations; including common-source, common-drain, and common-gain. The same evaluation would require three different two-port test-fixtures.

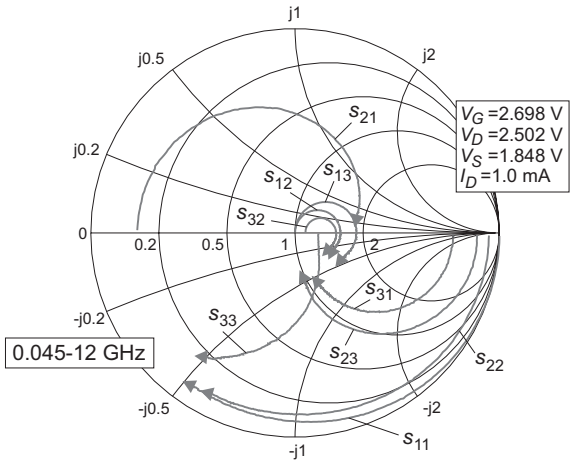

Fig. 7. Measured scattering parameters of 200×0.25 μm MOSFET.

V. Application of Measurements

To demonstrate the difference between the use of two-port and three-port measurements, the inductively degenerated LNA shown in Fig. 8 was designed for operation at 2 GHz using measured two-port network parameters. The simulated return loss of the circuit without inclusion of inductor parasitics is shown in Fig. 8. With the measured two-port network parameters the input match at 2 GHz is perfect. When simulating the exact same circuit using three-port measurements of the device with proper bias conditions, the input match is affected to a degree where a redesign is necessary. The importance of these aspects has recently been demonstrated with VSWR measurements on a differential CMOS RF amplifier [8].

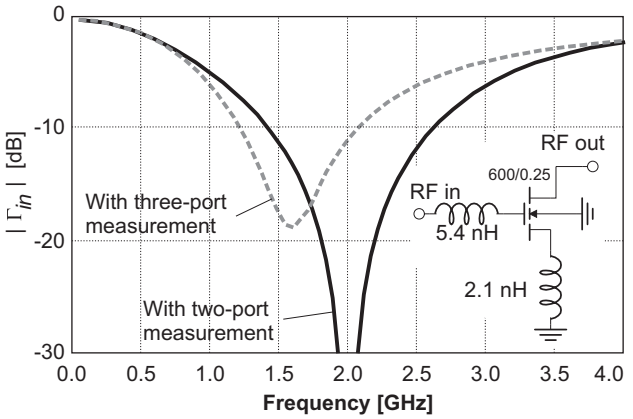

Fig. 8. Simulated return loss of LNA circuit using two-port and three-port measurements.

VI. Conclusions

In this paper, we have demonstrated an on-wafer characterization procedure for three-port devices. Using shield-based test-fixtures, we reduce port-port coupling and dangling leg impedance to an extent where low-complexity de-embedding is facilitated. Measurements display a high level of consistency, even when a two-port network analyzer is used. The advantage of using three-port network parameters over two-port parameters for accurately modeling circuit responses was clearly demonstrated using an RF CMOS design example.

References

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